Subject Code	Subject Name	Teaching Scheme			Credit Assigned		
		Theory	Pract.	Tut.	Theory	TW	Total
SEITC403	Computer Organization and Architecture	03	-	01	03	01	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				TW	Pract	Oral	Total
		Internal Assessment			End Semester Exam				
		Test1(T1)	Test2(T2)	Average of T1 & T2					
SEITC403	Computer Organization and Architecture	20	20	20	80	25	-	25	150

Pre-requistes: Fundamentals of Computer, Digital Logic Circuits, Programming Languages (C, C++, Java)

Course Educational Objectives (CEO):

CEO 1	To conceptualize the basics of organizational and architectural issues of a digital computer.
CEO 2	To analyze performance issues in processor and memory design of a digital computer.
CEO 3	To understand various data transfer techniques in digital computer.
CEO 4	To analyze processor performance improvement using instruction level parallelism

Course Learning Outcomes:

A	Ability to understand basic structure of computer.
B	Ability to perform computer arithmetic operations.
C	Ability to understand control unit operations.
D	Ability to design memory organization that uses banks for different word size operations.
E	Ability to understand the concept of cache mapping techniques.
F	Ability to understand the concept of I/O organization.
G	Ability to conceptualize instruction level parallelism.

Detail Syllabus:

Module	Detailed Contents	Hours
1	**Overview of Computer Architecture & Organization:** Introduction of Computer Organization and Architecture. Basic organization of computer and block level description of the functional units. Evolution of Computers, Von Neumann model. Performance measure of Computer Architecture. Introduction to buses and connecting I/O devices to CPU and Memory, bus structure.	04
2	**Data Representation and Arithmetic Algorithms:** Number representation: Binary Data representation, two's complement representation and Floating-point representation. IEEE 754 floating point number representation. Integer Data computation: Addition, Subtraction. Multiplication: Signed multiplication, Booth's algorithm. Division of integers: Restoring and non-restoring division Floating point arithmetic: Addition, subtraction	10
3	**Processor Organization and Architecture:** CPU Architecture, Register Organization , Instruction formats, basic instruction cycle. Instruction interpretation and sequencing. Control Unit: Soft wired (Micro-programmed) and hardwired control unit design methods. Microinstruction sequencing and execution. Micro operations, concepts of nano programming.Introduction to RISC and CISC architectures and design issues. Case study on 8085 microprocessor: Features, architecture, pin configuration and addressing modes.	12
4	**Memory Organization:** Introduction to Memory and Memory parameters. Classifications of primary and secondary memories. Types of RAM and ROM, Allocation policies, Memory hierarchy and characteristics. Cache memory: Concept, architecture (L1, L2, L3), mapping techniques. Cache Coherency, Interleaved and Associative memory. Virtual Memory: Concept, Segmentation and Paging , Page replacement policies.	12
5	**I/O Organization and Peripherals:** Input/output systems, I/O modules and 8089 IO processor. Types of data transfer techniques: Programmed I/O, Interrupt driven I/O and DMA. Peripheral Devices: Introduction to peripheral devices, scanner, plotter, joysticks, touch pad.	6
6	**Introduction to parallel processing systems:** Introduction to parallel processing concepts, Flynn's classifications, pipeline processing, instruction pipelining, pipeline stages, pipeline hazards.	4

Text Books:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", Fifth Edition, Tata McGraw-Hill.
2. John P. Hayes, "Computer Architecture and Organization", Third Edition.
3. William Stallings, "Computer Organization and Architecture: Designing for Performance", Eighth Edition, Pearson.
4. B. Govindarajulu, "Computer Architecture and Organization: Design Principles and Applications", Second Edition, Tata McGraw-Hill.

Reference Books:

1. Dr. M. Usha, T. S. Srikanth, "Computer System Architecture and Organization", First Edition, Wiley-India.
2. "Computer Organization" by ISRD Group, Tata McGraw-Hill.
3. Ramesh Gaonkar, "Microprocessor Architecture, Programming and Applications with the 8085, Fifth Edition,Penram.

Oral examination will be based on the above syllabus.

There will be at least eight assignments covering the above syllabus.

Term Work: 25 Marks (Total marks) = 20 Marks (Tutorials) + 5 Marks (Attendance)

Note: The faculty should conduct tutorials based on the above syllabus including two case studies on recent developments covering the above contents.
8085 microprocessor should be included only as a sample case study. No questions in University Exams / Class Tests should be asked on 8085 microprocessor.

SUGGESTED LIST OF ASSIGNMENTS FOR COA TUTORIALS:

1. To study Full Adder (7483).
2. To study ALU (74181).
3. To study MASM (Micro Assembler).
4. A program for hexadecimal addition and multiplication.
5. A program for binary multiplication.
6. A program for Hamming code generation , detection and correction.
7. A program for Booth's multiplication
8. A program for LRU page replacement algorithm.
9. A program for FIFO page replacement algorithm.
10. To study mapping techniques of Cache memory.
    10.1 Direct Mapped cache
    10.2 Associative Mapped cache
    10.3 Set Associative Mapped cache

11. To study memory allocation policies.
    11.1 First-fit algorithm
    11.2 Best-fit algorithm

12. A program to implement serial communication (PC - PC communication).
13. A program to implement parallel communication. (PC - Printer communication).

Theory Examination:

- Question paper will comprise of 6 questions, each carrying 20 marks.
- Total 4 questions need to be solved.
- Q.1 will be compulsory, based on entire syllabus wherein sub questions of 2 to 3 marks will be asked.
- Remaining question will be randomly selected from all the modules.

Weightage of marks should be proportional to number of hours assigned to each module.