Course Code	Course Name	Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ITL301	Digital Design Lab	--	2	--	--	1	--	01

Course Code	Course Name	Examination Scheme						
		Theory Marks				Term Work	Oral & Practical	Total
		Internal assessment			End Sem. Exam			
		Test1	Test2	Avg. of two Tests				
ITL301	Digital Design Lab	--	--	--	--	25	25	50

Lab Objectives: Students will try to:

1. Learn to minimize and design combinational logic;
2. Understand the relationships between combination logic and Boolean algebra, and between sequential logic and finite state machines;
3. Appreciate tradeoffs in complexity and speed of combinational designs;
4. Understand how state can be stored in a digital logic circuit;
5. Study how to design a simple finite state machine from a specification and be able to implement this in gates and edge triggered flip-flops
6. Learn to translate real world problems into digital logic formulations

Lab Outcomes: Students will be able to:

1. Minimize the Boolean algebra and design it using logic gates.
2. Analyse and design combinational circuit.
3. Realise given function using combinational circuit.
4. Design and develop sequential circuits
5. Implement digital systems using programmable logic devices
6. Translate real world problems into digital logic formulations using VHDL.

Prerequisite: Concepts of Logic Design

Hardware requirement:

Digital Trainer kit, ICs for various logic gates and functions, connecting wires

Software requirement:

VHDL tool

Detail Syllabus:

Sr. No.	**Module**	Detailed Content	**Hours**	**LO Mapping**

I	Boolean Algebra and Logic gates	a. Verify the truth table of logic gates (basic and universal gates) b. Realization of Boolean algebra using gates	04	LO1
II	Design and Analysis of Combinational Circuits	a. Design of Full Adder and Full Subtractor. b. verify the operation of 4- bit magnitude comparator	04	LO2
III	Implementation of Combinational Circuits	a. Implementation of MUX and DeMUX. b. Implementation of Encoder and Decoder	04	LO3
IV	Sequential Logic Design	a. To verify and observe the operation of flip-flop(any two) b. To design any two shift register. c. To design Modulo and ring Counter	06	LO4
V	Programmable logic Devices	a. Evaluate and observe Boolean expression using PALs and PLAs..	04	LO5
VI	VHDL	a. Implementation of Logic Gates using VHD b. Evaluate and observe combinational circuits on VHDL.	04	LO6

Text Books:

1. R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill.
2. Balbaniam,Carison,”Digital Logic Design Principles”, Wiley Publication

References:

1. M. Morris Mano, “Digital Logic and computer Design”, PHI
2. J. Bhasker.“ VHDL Primer”, Pearson Education.

Term Work:
Term Work shall consist of at least 10 to 12 practical’s based on the above list. Also Term work Journal must include at least 2 assignments.
Term Work Marks: 25 Marks (Total marks) = 15 Marks (Experiment) + 5 Marks (Assignments) + 5 Marks (Attendance)

Oral & Practical Exam: An Oral & Practical exam will be held based on the above syllabus.